AF/2816 $4

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor(s): Eduard Sackinger

Case: Sackinger 8

Serial No.: 09/498,559 **Group Art Unit:** 2816

Filed: February 4, 2000

Examiner: D. Le

Title: Active Inductor

THE COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

SIR:

Enclosed is an Appellant's Brief Under 37 C.F.R. 1.192 Before the Board of Patent Appeals and Interferences in the above-identified appeal.

Please charge the amount of $330.00, covering payment of the fee for the Appeal Brief, to **Lucent Technologies Inc. Deposit Account No. 12-2325**. In the event of any non-payment or improper payment of a required fee, the Commissioner is authorized to charge Deposit Account No. 12-2325 as required to correct the error.

Respectfully submitted,

By Eugene J. Rosenthal

Eugene J. Rosenthal
Reg. No. 36,658
Area Code (732) 949-1857

Date: FEB. 25, 2004

Lucent Technologies Inc.
Docket Administrator
101 Crawfords Corner Road (Room 3J-219)
Holmdel, New Jersey 07733

Certificate of Mailing

I hereby certify that this correspondence (and any paper referred to as being transmitted therewith) is being deposited with the United States Postal Service with sufficient postage as First Class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313 on the date indicated below:

FEB. 25, 2004
Date

Sharon Lobosco
SHARON LOBOSCO

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Inventor(s):	Eduard Sackinger		
Case:	8		
Serial No.:	09/498,559	**Group Art Unit:**	2816
Filed:	February 4, 2000		
Examiner:	D. Le		
Title:	Active Inductor		

THE COMMISSIONER OF PATENTS AND TRADEMARKS
WASHINGTON, D. C. 20231

SIR:

Appellant's Brief Under 37 C.F.R. 1.192

This is an appeal to the Board of Patent Appeals and Interferences from the Final Rejection dated June 30, 2003. Applicants are submitting this Brief in triplicate.

A Notice of Appeal was timely filed.

Real Party in Interest

The real party in interest is Lucent Technologies Inc.

Related Appeals and Interferences

There are no related appeals or interferences.

Status of Claims

Claims 1-19, which are pending in this application, stand finally rejected. A copy of the claims under appeal as now presented are appended to this brief in Appendix A.

Status of Amendments

All amendments to the claims have been entered.

Summary of the Invention

As is well known, inductors can be used to expand the bandwidth of amplifiers. When an amplifier requiring an inductor is implemented on an integrated circuit, the inductor may be implemented either as spiral inductor or as an active inductor. The problems with using a spiral inductor are a) a spiral inductor is large, and b) the useful frequency range of spiral inductors is limited by self resonance. Although active inductors are small, and they typically have a greater frequency range than a spiral inductor, active inductors suffer from the problem of requiring a relatively large voltage drop, with respect to the power supply voltage, across the active inductor. With power supply voltages decreasing, to reduce power consumption, the relatively large voltage drop of prior art active inductors becomes problematic, in that it does not leave enough headroom for the amplifying circuit coupled to the active inductor to operate properly.

A better active inductor that performs better than prior art active inductors on integrated circuits that are supplied with the same power supply voltage can be realized, in accordance with the principles of the invention, by biasing the active inductor from a voltage higher than the power supply voltage, with the higher-than-the-power-supply voltage being generated on the integrated circuit. Advantageously, more headroom is left for the amplifying circuit coupled to the active inductor to operate properly than with prior art active inductors. Furthermore, by not simply operating the entire active inductor from a higher voltage, the power dissipation remains the same as if the active inductor were connected as in the prior art only to the power supply voltage, and the task of generating the voltage higher than the power supply voltage is simplified, because only leakage current, e.g., nanoamps, is required.

Grouping of Claims

Claims 1-19 are apparatus claims. Claims 1, 14, and 16 are independent claims. For purposes of this appeal, claims 1-13 and claims 14-19 stand as separate groups, since each such group is rejected based on different art.

Issues

I. Are claims 14-19 properly rejected under 35 U.S.C. 102(b) as being anticipated by United States Patent No. 6,069,516 issued to Vargha on May 30, 2000.

II. Are claims 1-13 properly rejected under 35 U.S.C. 103(a) as being unpatentable over Vargha in view of United States Patent No. 6,028,496 issued to Ko et al. on February 22, 2000.

Arguments

Issue I – Rejection of Claims 14-19 under 35 U.S.C. 102(b)

In essence, the Office Action alleges that Vargha has the same structure as applicants' claims and that applicants' claims do not limit the mode of operation to that of an active inductor. By contrast, applicants argue that the structure of Vargha is different, because it is lacking a necessary resistor—which is included applicants' arrangement—that is necessary to properly bias the MOSFET of Vargha to act as inductor. Thus, although Vargha may appear at first glance to be very similar to, or the same as, applicants' invention, nevertheless, the circuit of Vargha is not an active inductor. Moreover, the circuit of Vargha does not meet the recitiation of applicants' claim that the "MOS transistor is coupled to said beyond voltage generator so as to bias said MOS transistor with said beyond voltage and said MOS transistor is adapted to operate as said active inductor".

More specifically, the Office Action States that Vargha discloses a circuit comprising a transistor and a charge pump. Thus, Vargha has the same structure as applicants' claims. Furthermore, the Office Action notes that applicant's previously argued that the circuit of Vargha does not operate as an inductor. This argument, the Office Action states, is not persuasive, because, according to the Office Action, there is nothing stated in the rejected claims as to how to properly bias the transistor for the correct mode of operation. Instead, the Office Action asserts that the claims simply recite that the gate of the transistor is coupled to a power supply voltage having an absolute value larger than the first power supply voltage, and such a limitation is shown in Figure 1 of Vargha.

However, the Office Action's circuit analysis and conclusion that the circuit of Vargha inherently operates as an inductor is scientifically incorrect. Rather, the circuit of Varhga does **NOT** operate as an inductor!

The Office Action seems to believe that any transistor biased by a voltage beyond the power supply can act as a gyrator transforming a capacitance in an inductance.

This is incorrect.

Only specific arrangements of circuit elements, e.g., transistors and resistors, can so act as gyrators. Furthermore, the transistor(s) must be properly biased for the correct mode of operation. In the case of the instant invention, the transistor must be biased for the saturation mode, in which it acts as a transconductor.

By contrast, as noted, the circuit of Vargha does **not** have a gate resistor connected to its transistor, nor is its transistor biased to operate in saturation. Consequently, Vargha does not form a gyrator. However, a gyrator is necessary to transform a capacitance—in the instant invention the gate-source capacitance—into an inductance. (Nor does Vargha teach or suggest the two coupled transconductors as in Ko et al., which is an alternative arrangement that could be used to form a gyrator and transform a capacitance into an inductance.)

For the transistor of Vargha to work as part of a gyrator it should operate as transconductor, which means that it must be biased, as is the instant invention, to satisfy

$V_{DS} > V_{GS} - V_{TH}$ and $V_{GS} > V_{TH}$ (saturation mode).

However, this is **not** the case in Vargha. Instead, the circuit of Varhga actually only operates as a switch. This is because the transistor of Vargha is biased to satisfy

$V_{DS} < V_{GS} - V_{TH}$ (ohmic mode); or

$V_{GS} < V_{TH}$ (off mode).

Therefore, even though at first glance Vargha may seem to resemble applicant's invention, this is merely a surface resemblance. Analysis of the circuits' actual operation reveals that Vargha really in no way resembles applicant's invention, nor does it suggest same.

Each of applicants' independent claims 14 and 16 require that the transistor be biased so as to be operated as an inductor.

More specifically, claim 14 states: "said MOS transistor is coupled to said beyond voltage generator so as to **bias** said MOS transistor with said beyond voltage **and** said MOS transistor is adapted to operate as said active inductor". This language means that the MOS transistor claimed by applicant is biased by the beyond voltage—which is a voltage outside the range of the voltage supplied by a power supply—in such a manner so as to operate as an active inductor. In other words, there are two conditions required by the claim language, 1) that the MOS transistor be biased using the beyond voltage and 2) that this biasing be done in to cause the MOS transistor to operate as an active inductor. The transistor of Vargha never acts as an active inductor, nor can it ever, given the biasing arrangement it has.

Claim 16 states: "a metal oxide semiconductor (MOS) transistor adapted to operate as an active inductor that is biased using a voltage generated on said integrated circuit that is outside the range of the voltage supplied by a power supply". Although the wording is slightly different, this language, as in claim 14, means that the MOS transistor claimed by applicant is biased by the voltage outside the range of the voltage supplied by a power supply in such a manner so as to be operated as an active inductor. The same two conditions required by claim 14 are also required by the claim language of claim 16, namely, 1) that the MOS transistor be biased using a voltage outside the range of the voltage supplied by a power supply and 2) that this biasing be done in to cause the MOS transistor to operate as an active inductor. The transistor of Vargha never acts as an active inductor, nor can it ever, given the biasing arrangement it has.

Thus, applicants' independent claims 14 and 16 are allowable over Vargha under 35 U.S.C. 102(b).

Issue II – Rejection of Claims 1-13 under 35 U.S.C. 103(a)

Claims 1-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Vargha in view of United States Patent No. 6,028,496 issued to Ko et al. on February 22, 2000.

The Office Action states that Vargha discloses all of the limitations of the claimed invention but does not disclose a resistor. However, continues the Office Action, Ko et al., teach a circuit comprising resistors (R2-R8) for reducing rush current to the transistors

in order to protect these transistors. Therefore, concludes the Office Action, it would have been obvious to a person of ordinary skill in the art to employ the resistor as taught by Ko et al. in the circuit of Vargha for purpose of protecting the transistor.

Applicant respectfully traverses this ground of rejection for the following reasons.

Notwithstanding, one would **not** combine Vargha and to Ko et al., and it is clear that one should **not** do so.

The biasing regimes of Vargha and Ko et al. are mutually exclusive. Either the biasing is arranged as in Vargha, so that the circuit operates as a switch, with the active element, i.e., the transistor, being either in Ohmic mode or off mode, or the biasing is arranged as in Ko et al., to produce a gyrator for use in an active inductor.

To do as the Office Action suggests, i.e., to insert the resistors of Ko et al. into the circuit of Vargha, would **not** produce an active inductor.

The Office Action's suggestion seems to be based on the similarity of the pictures and hindsight from applicant's invention, not on an actual electrical function analysis of the circuits at issue. However, the motivation of one of ordinary skill in the art would come only from a correct electrical function circuit analysis.

In the instant invention, the resistor at issue is part of the gyrator which transforms a capacitance into an inductance. The resistor is **not** for the purpose of protection against rush current. More specifically, applicant employs a) a transistor, which acts as a transconductor, and b) a gate resistor, to form a gyrator.

With regard to Ko et al., the Office Action assumes that R2, R4, R6, and R8 perform some "protection" function from a rush current from the voltage source Vdd. This appears to be incorrect. Nowhere in Ko et al. does it state that such is the function of those resistors. Additionally, there is no mention of protection or of rush current. Ascribing such resistors a protection function appears to be solely based on a sua sponte analysis by the Office Action of the figure of Ko et al. without regard for the explanation given explicitly in Ko et al. of the function of these resistors. However, in Ko et al. it is clear from column 3, line 42 through column 4, line 12 that the function of the resistors is related to biasing the active elements of the circuit. To wit:

The **biasing** portion 40 of FIG. 2, corresponding to the biasing portion 10 of FIG. 1, includes a fourth transistor MT4 having a drain and a source connected between a first supply power V_{dd} and the input signal V1, a third capacitor C3 connected between the input signal V1 and the gate of the fourth transistor MT4, a first resistor R1 having a first end connected to the first supply power V_{dd}., a second resistor R2 connected between a second end of the first resistor R1 and the gate of the fourth transistor MT4, a third resistor R3 having a first end connected to the second end of the first resistor R1, a fourth resistor R4 connected between a second end of the third resistor R3 and a gate of the third transistor MT3, a fifth resistor R5 having a first end connected to the second end of the third resistor R3, a sixth resistor R6 connected between the second end of the fifth resistor R5 and a gate of the second transistor MT2, a seventh resistor R7 having a first end connected to the second end of the fifth resistor R5, an eighth resistor R8 connected between the second end of the seventh resistor R7 and the gate of the first transistor MT1, and a ninth resistor R9 connected between the second end of the seventh resistor R7 and a second supply power V_{gg}.

The conventional active inductors described above have a small gate capacitance, in other words, high impedance, so that a **bias** resistance of 6 k Ω or greater is required to access each gate. It is therefore difficult to use a resistor chain including the resistors R1, R3, R5, R7 and R9 shown in FIG. 2, and many pins are required. However, in the first preferred embodiment of the present invention, a **bias signal** is applied to each gate of the transistors **via the resistor chain**, and the resistors R2, R4, R6 and R8 are connected to each resistor of the resistor chain to reduce the number of **bias** pins. In the end, the first preferred embodiment of FIG. 2 can readily change the **bias** current and stabilize the bias at the same time, as described in I. D. Robertson et al., "Ultrawideband biasing of MMIC distributed amplifiers using improved active load," Electronics Letters, Vol. 27, No. 21, pp. 1907-1909 (1991). (Emphasis added)

Given that the function ascribed to the resistors by the Office Action is **not** correct, i.e., there is **no** protection function, so too the motivation ascribed to one of

ordinary skill in the art by the Office Action to combine such resistors with the circuit of Vargha based on that function is can**not** be correct.

Furthermore, even if the Office Action were correct in ascribing to R2 of Ko et al. a function of protecting against a rush current from Vdd, why would one want to combine Ko et al. with Vargha, the result of which would, according to the Office Action's combination, place a greater voltage at the input to R2, thereby causing an even greater rush current. Clearly to do so is contraindicated by the Office Action's own reasoning. Moreover, it seems clear from the lack of any discussion about it in Vargha, where there is no protection resistor provided, that there is **no** problem with rush current in its switch circuit, and hence there is **no** motivation to introduce therein any form of "protection".

To reiterate, the resistors of Ko et al. do **NOT** serve to protect the MOSFET, but to **bias** it for proper operation as an active inductor. The Office Action's suggestion that the resistors serve an additional or alternative function of protection reads nicely and may appear, at first glance, seductive in an Office Action. However, actually, it is based on a misunderstanding of the circuit in Ko et al. and a complete mischaracterization of the circuit's nature and the function of the resistors. Therefore, one of ordinary skill in the art would **not**, for any considered reason, combine the Vargha and Ko et al. references if merely given the Vargha and Ko et al. references. Hence there is **no** rational upon which an obviousness rejection using the Vargha and Ko et al. references can be based.

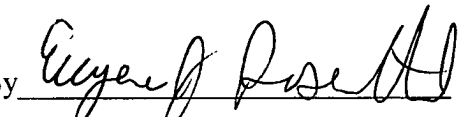
Since there is no teaching, suggestion, or motivation to combine Vargha with Ko et al., doing so is an improper basis for a rejection, and applicants claims 1-13 are allowable over Vargha and Ko et al. applicant's claims are allowable over the suggested combination.

Conclusion

In view of the foregoing, it is submitted that the Examiner is in error. It is, accordingly, respectfully requested that the rejection of claims 1-19 be reversed and the application passed to issue.

Respectfully,

Eduard Sackinger

By 

Eugene J. Rosenthal, Attorney
Reg. No. 36,658
732-949-1857

Lucent Technologies Inc.

Date: FEB. 25, 2004

APPENDIX A

Claims

1. A circuit for use as an active inductor on an integrated circuit having a power supply voltage supplied at a first power supply terminal, comprising:

an metal oxide semiconductor (MOS) transistor having a gate terminal, a drain terminal, and a source terminal, said drain terminal being coupled to said power supply voltage and said source terminal being one of the terminals of said active inductor; and

a resistor having a first terminal coupled to said gate terminal and a second terminal coupled to a voltage that is derived from said power supply voltage and has a larger absolute value than said power supply voltage supplied at said first power supply terminal and the same sign as said power supply voltage;

said circuit being adapted so that when said circuit is operating said circuit behaves as an active inductor between said source terminal and an other terminal of said active inductor on said integrated circuit.

2. The invention as defined in claim 1 wherein other terminal of said active inductor is said first power supply terminal.

3. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal.

4. The invention as defined in claim 1 wherein MOS transistor is a negative metal oxide semiconductor (NMOS) transistor.

5. The invention as defined in claim 1 wherein MOS transistor is a positive metal oxide semiconductor (PMOS) transistor.

6. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is higher than a voltage supplied from said second power supply terminal.

7. The invention as defined in claim 1 wherein said MOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said power supply voltage supplied from said first power supply terminal is lower than a voltage supplied from said second power supply terminal.

8. The invention as defined in claim 1 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS) transistor, said NMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the positive power supply terminal for said integrated circuit and said second power supply terminal is the negative power supply terminal for said integrated circuit.

9. The invention as defined in claim 1 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS) transistor, said PMOS transistor also has a bulk terminal, said bulk terminal being connected to a second power supply terminal, and wherein said first power supply terminal is the negative power supply terminal for said integrated circuit and said second power supply terminal is the positive power supply terminal for said integrated circuit.

10. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage and has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage has a larger absolute value than said power supply by one threshold voltage of said MOS transistor.

11. The invention as defined in claim 1 wherein said voltage that is derived from said power supply voltage is generated from said power supply voltage by a high voltage generator.

12. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

13. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage, said high voltage generator comprising:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a signal that has an average larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

and a ripple filter which filters said output of said clamp and supplies the output of said high voltage generator, which said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

14. (Amended) A circuit for use as an active inductor on an integrated circuit, comprising:

a metal oxide semiconductor (MOS) transistor; and

a beyond voltage generator which generates a beyond voltage that is either greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

wherein said MOS transistor is coupled to said beyond voltage generator so as to bias said MOS transistor with said beyond voltage and said MOS transistor is adapted to operate as said active inductor.

13. The invention as defined in claim 1 further including on said integrated circuit a high voltage generator that generates said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage, said high voltage generator comprising:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a signal that has an average larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage;

and a ripple filter which filters said output of said clamp and supplies the output of said high voltage generator, which said voltage that has a larger absolute value than said power supply voltage supplied by said first power supply terminal and the same sign as said power supply voltage.

14. A circuit for use as an active inductor on an integrated circuit, comprising:

a metal oxide semiconductor (MOS) transistor; and

a beyond voltage generator which generates a beyond voltage that is either greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

wherein said MOS transistor is coupled to said beyond voltage generator so as to bias said MOS transistor with said beyond voltage and said MOS transistor is adapted to operate as said active inductor.

15. The invention as defined in claim 14 wherein said beyond voltage generator comprises:

an oscillator generating an oscillating output signal;

a voltage doubler receiving as an input said oscillating output signal from said oscillator and supplying as an output a voltage signal that has an average voltage that is either greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

a clamp which receives as an input said output of said voltage doubler and supplies an output voltage substantially clamped to a prescribed value that is greater than the highest voltage or less than the lowest voltage being supplied to said integrated circuit by a power supply;

and a ripple filter which filters said output of said clamp and supplies the output of said beyond voltage generator.

16. An integrated circuit comprising a metal oxide semiconductor (MOS) transistor adapted to operate as an active inductor that is biased using a voltage generated on said integrated circuit that is outside the range of the voltage supplied by a power supply off of said integrated circuit for operating said integrated circuit.

17. The invention as defined in claim 16 wherein said MOS transistor is a negative metal oxide semiconductor (NMOS) transistor.

18. The invention as defined in claim 16 wherein said MOS transistor is a positive metal oxide semiconductor (PMOS) transistor.

19. The invention as defined in claim 16 wherein said active inductor is biased by coupling a gate of said MOS transistor to said voltage generated on said integrated circuit that is beyond the range of the voltage supplied by a power supply for operating said integrated circuit via an impedance.